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THE ROLE OF THE NIOS II SOFT-CORE PROCESSOR IN THE DESIGN OF DIGITAL DEVICES

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Abstract: This paper examines where the 32-bit Nios II soft-core processor, developed by Intel (Altera), fits into the design of modern digital devices and why it matters. We look at the flexibility of its architecture, at what it offers for building a system-on-chip (SoC), and at the possibility of accelerating instructions directly in hardware through Custom Instructions. Conventional microcontrollers are then compared with systems built around a soft-core processor, and the paper closes with recommendations for making the design process more efficient.

Key words: FPGA, programmable logic device (PLD), Nios II, soft-core processor, Platform Designer, Avalon bus, Custom Instructions, SoC, digital systems.

Introduction

Microprocessor and digital system design is changing fast. Conventional microcontrollers (MCUs) and digital signal processors (DSPs) still handle many routine tasks well enough. Once an application needs high throughput, parallel processing, or a great deal of flexibility, however, their limits become apparent. It is in this niche that field-programmable gate arrays (FPGAs), also called programmable logic integrated circuits, have emerged as the most promising basis for digital design.

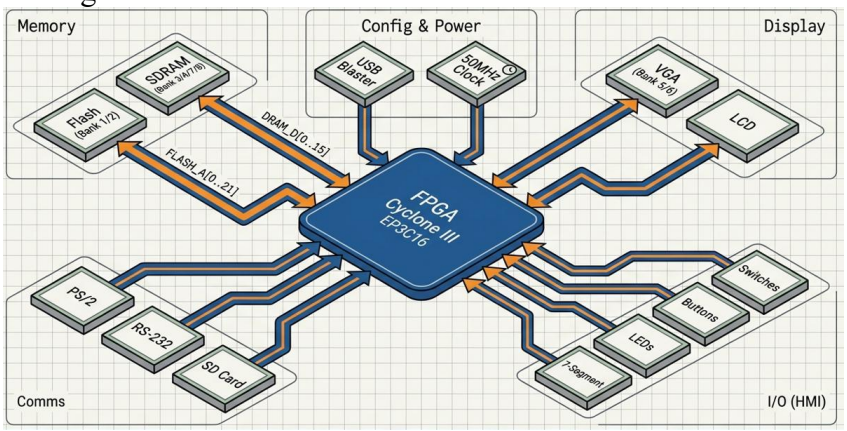


Figure 1. Architecture of the Cyclone III FPGA and the structure of its internal logic blocks.

Soft-core processors, built in software inside the FPGA itself, have pushed the combination of hardware and software a step further. Intel's Nios II is a prominent example. With it, a designer can place fast logic circuits and a processing core capable of running complex algorithms on one semiconductor die. The practical gains are smaller devices, lower cost, and a marked increase in performance.

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Nios II is a 32-bit soft-core processor with a RISC (Reduced Instruction Set Computer) architecture, designed specifically for Intel (formerly Altera) FPGAs. A hard-core processor arrives as finished silicon. Nios II does not. It exists as design code in a hardware description language (VHDL or Verilog) and is realized from the FPGA's own logic elements (LEs).

System-on-a-chip (SoC) integration. What makes Nios II so valuable in digital design is, above all, its tight integration with the SOPC (System on a Programmable Chip) environment, now known as Intel Platform Designer (formerly Qsys). Working from a library of ready-made blocks, a designer can put together an entire computer system with a custom architecture in a matter of minutes. The central processor, timers, UART ports and memory controllers are all linked by the high-bandwidth Avalon Switch Fabric. Two bus interfaces are used in a Nios II system: Avalon Memory-Mapped (MM) and Avalon Streaming (ST). The first serves addressable devices and memory. The second carries high-speed streaming data, such as video or digital signals, straight between peripherals, so the processor does not have to handle it.

Hardware acceleration (Custom Instructions). Run in software, in C or C++, complex mathematical algorithms, cryptographic operations and digital signal processing (DSP) routines can consume hundreds or even thousands of clock cycles. Nios II addresses this through its extensible set of arithmetic and logic instructions, known as Custom Instructions, which is among its defining features. The designer takes a given function, for instance a Fourier transform, a matrix multiplication or the AES encryption algorithm, and implements it as a dedicated block that runs in parallel on the FPGA's logic elements. The block is wired directly into the arithmetic logic unit (ALU) of the Nios II. From the software side, one line of C is enough to call it, and computational efficiency can rise by a factor of 100 to 500.

Development environment. With the hardware in place, the project moves on to software. Development for Nios II is fully automated and follows current programming practice. The Intel Nios II Software Build Tools (SBT) are based on the popular Eclipse IDE and allow code to be written and debugged in C and C++. A Hardware Abstraction Layer (HAL) is also provided. Because of it, the designer need not manipulate the internal registers of peripheral devices directly and can use standard calls such as printf() and fopen(). For managing complex concurrent tasks, real-time operating systems (RTOS) such as MicroC/OS-II or FreeRTOS run on Nios II without difficulty.

Nios II is already used in a wide variety of digital systems. The main areas are the following:

- **Industrial automation and robotics:** precise control of motors and fast analysis of sensor data.
- **Telecommunications equipment:** routing, packet sorting, and protocols for high-speed data transfer.
- **Medical diagnostic equipment:** real-time digital processing of X-ray, ultrasound and other medical images.
- **Aerospace and military systems:** dependable, stable computation in radar systems and satellite hardware.

Conclusion

To sum up, the Nios II soft-core processor plays a very important part in the design of digital devices. It brings together two things that are normally separate: the flexible software control of a conventional microcontroller and the fast, parallel hardware processing of an FPGA. Custom Instructions and the Avalon interfaces allow a system to be tuned to a high degree, shorten development time and reduce cost. For these reasons Nios II remains one of the most dependable and effective tools for building modern, technology-intensive systems.

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